Amendments to the Claims

This listing of claims will replace all prior version, and listings, of the claims in the application:

Listing of Claims:

Claim 1 (currently amended) A hybrid content addressable memory array comprising:

a first memory portion having a first type of content addressable memory cells arranged in rows and columns, each of the first type of content addressable memory cells including search and compare stacks for coupling a matchline to a tail line if search data matches stored data;

a second memory portion having a second type of content addressable memory cells arranged in rows and columns, the second type of content addressable memory cells being electrically coupled to the first type of content addressable memory cells, each second type of content addressable memory cell being smaller in size than each first type of content addressable memory cell, the second memory portion being operable simultaneously with the first memory portion.

Claim 2 (Original) The hybrid content addressable memory array of claim 1, wherein the first memory portion and the second memory portion include matchlines, each matchline of the first memory portion being coupled to the first type of content addressable memory cells, and each matchline of the second memory portion being coupled to the second type of content addressable memory cells.

Claim 3 (Original) The hybrid content addressable memory array of claim 2, wherein the first type of content addressable memory cells include ternary content addressable memory cells and the second type of content addressable memory cells include binary content addressable memory cells.

Claim 4 (Original) The hybrid content addressable memory array of claim 3, wherein the matchlines of the first memory portion and the matchlines of the second memory portion are interleaved with each other.

Claim 5 (Cancelled)

Claim 6 (Cancelled)

Claim 7 (previously presented) The hybrid content addressable memory array of claim 3, wherein the ternary content addressable memory cells include SRAM based ternary content addressable memory cells.

Claim 8 (previously presented) The hybrid content addressable memory array of claim 3, wherein the binary content addressable memory cells include SRAM based binary content addressable memory cells.

Claim 9 (Original) The hybrid content addressable memory array of claim 1, wherein at least one of the first and the second type of content addressable memory cells include configurable ternary-binary content addressable memory cells.

Claim 10 (Original) The hybrid content addressable memory array of claim 1, wherein the first type of content addressable memory cells and the second type of content addressable memory cells of a row are coupled to a logical matchline.

Claim 11 (Original) The hybrid content addressable memory array of claim 10, wherein the logical matchline includes a segmented matchline.

Claim 12 (Original) The hybrid content addressable memory array of claim 11, wherein the segmented matchline includes a first matchline segment and a second matchline segment.

Claim 13 (Original) The hybrid content addressable memory array of claim 12, wherein the first type of content addressable memory cells are coupled to the first matchline segment and the second type of content addressable memory cells are coupled to the second matchline segment.

Claim 14 (Original) The hybrid content addressable memory array of claim 1, wherein the first type of content addressable memory cells and the second type of content addressable memory cells of a column are coupled to common searchlines.

Claim 15 (currently amended) A hybrid content addressable memory array comprising:

a first type of content addressable memory cells coupled to a logical matchline, each of the first type of content addressable memory cells including search and compare stacks for coupling the logical matchline to a tail line if search data matches stored data; and

a second type of content addressable memory cells coupled to the logical matchline, and being operable simultaneously with the first type of content addressable memory cells, each second type of content addressable memory cell being smaller in size than each first type of content addressable memory cell.

Claim 16 (previously presented) The hybrid content addressable memory array of claim 15, wherein the first type of content addressable memory cells include ternary content addressable memory cells and the second type of content addressable memory cells include binary content addressable memory cells.

Claim 17 (previously presented) The hybrid content addressable memory array of claim 16, wherein the ternary content addressable memory cells include SRAM based ternary content addressable memory cells and the binary content addressable memory cells include SRAM based binary content addressable memory cells.

Claim 18 (Original) The hybrid content addressable memory array of claim 15, wherein the logical matchline includes a segmented matchline.

Claim 19 (Original) The hybrid content addressable memory array of claim 18, wherein the segmented matchline includes at least two matchline segments.

Claim 20 (Original) The hybrid content addressable memory array of claim 19, wherein the first type of content addressable memory cells are coupled to one of the at least two matchline segments and the second type of content addressable memory cells are coupled to the other of the at least two matchline segments.

Claim 21 (currently amended) A hybrid content addressable memory array comprising:

a first type of content addressable memory cells coupled to common searchlines, each of the first type of content addressable memory cells including search and compare stacks for coupling a matchline to a tail line if search data of the common searchlines matches stored data; and

a second type of content addressable memory cells coupled to the common searchlines and being operable simultaneously with the first type of content addressable memory cells, each second type of content addressable memory cell being smaller in size than each first type of content addressable memory cell.

Claim 22 (previously presented) The hybrid content addressable memory array of claim 21, wherein the first type of content addressable memory cells include ternary content addressable memory cells and the second type of content addressable memory cells include binary content addressable memory cells.

Claim 23 (previously presented) The hybrid content addressable memory array of claim 22, wherein the ternary content addressable memory cells include SRAM based ternary content addressable memory cells and the binary content addressable memory cells include SRAM based binary content addressable memory cells.

Claim 24 (New) The hybrid content addressable memory array of claim 1, wherein each search and compare stack includes a compare transistor and a search transistor serially connected between the matchline and the tail line, the compare transistor gate receiving the stored data and the search transistor gate receiving the search data.

Claim 25 (New)The hybrid content addressable memory array of claim 24, wherein further including a second compare transistor and a second search transistor serially connected between the matchline and the tail line, the second compare transistor gate receiving complementary stored data and the second search transistor gate receiving complementary search data.

Claim 26 (New) The hybrid content addressable memory array of claim 1, wherein the stored data includes a first data bit and a second data bit, the search data includes a first search bit and a second search bit.

Claim 27 (New)The hybrid content addressable memory array of claim 26, wherein the search and compare stack includes a first compare transistor and a first search transistor serially connected between the matchline and the tail line, and a second compare transistor and a second search transistor serially connected between the matchline and the tail line, the first compare transistor gate receiving the first data bit, the second compare transistor gate receiving the second data bit, the first search transistor gate receiving the first search bit, and the second search transistor gate receiving the second search bit.

Claim 28 (New) The hybrid content addressable memory array of claim 26, wherein the search and compare stack includes a first compare transistor, a first search transistor, and a mask transistor serially connected between the matchline and the tail line, and a second compare transistor, a second search transistor, and the mask transistor serially connected between the matchline and the tail line, the first compare transistor gate receiving the first data bit, the second compare transistor gate receiving a complement of the first data bit, the first search transistor gate receiving the first search bit, the second search transistor gate receiving the second search bit, and the mask transistor receiving the second data bit.